CLAIMS

1. (withdrawn) A circuit for taking the square root of a square value, comprising:

a first register for storing a current estimate having an input and an output;

a first shifter having an input coupled to the output of the first register and an output;

a counter having an output;

a second shifter having an input coupled to the output of the counter and an output, wherein a shift amount is responsive to the output of the counter;

a first summer having a first input coupled to the output of the first shifter, a second input coupled to the output of the second shifter, and an output;

a third shifter having a first input coupled to the output of the summer, a second input coupled to the output of the counter, and an output;

a second summer having a first input coupled to the output of the third shifter, a second input, and an output;

a comparator having a first input coupled to the output of the second summer, a second input for receiving the square value, and an output coupled to the input of the first register;

a multiplexer having a first input coupled to the output of the second summer, a second input coupled to the second input of the second summer, a third input coupled to the output of the comparator; and an output; and

a second register having an input coupled to the output of the multiplexer and an output coupled to the second input of the second summer.

2. (withdrawn) The circuit of claim 1, further comprising a logic circuit having an input for receiving a clock circuit and an output coupled to the counter, the first register, and the second register.

3. (withdrawn) A method of performing an iteration for calculating a square root of a square value, comprising:

providing an estimate of the square root;

performing a left shift of one on the current estimate to form a first shifted output;

shifting a one by a counter amount to form a shifted one output;

adding the shifted one output to the first shifted output to form a first added number;

performing a left shift of the counter amount on the first added number to form a second shifted output;

adding the second shifted output to a square of the current estimate to form a squared estimate;

comparing the squared estimate to the square value to determine a state of an update output;

updating the current estimate and the square of the current estimate based on the update output.

4. (withdrawn) The method of claim 3, wherein the updating comprises changing the square of the current estimate to be equal to the squared estimate if the update output is in a first state and leaving the square of the current estimate unchanged if the update output is in a second state.

5. (withdrawn) In a method of calculating a square root by calculating bits of an estimated square root in descending order of significance in which the uncalculated bits are zero, a method for calculating a next bit comprising:

shifting the estimated square root in the direction of more significance by one to provide a shifted estimated square root;

providing a one at a bit location of a first number corresponding to the next bit to provide an iterative value;

adding the iterative value to the shifted estimated square root to provide a first added value;

shifting in the direction of more significance the added value by the first number to provide a shifted added value;

adding the shifted added value to a square of the estimated square root to provide an estimated squared value;

comparing the estimated squared value to the square value and providing an update output indicative of the comparison; and

applying a one as the next bit in the estimated square root if the update output is in a first state.

6. (currently amended) A method of performing an arithmetic function to achieve a result based on a number (square) on which the arithmetic function is performed, comprising

~~determining~~ storing a first partial iteration of the result in a first register;

performing an inverse of the arithmetic function on the first partial iteration to determine a first estimated inverse;

comparing the first estimated inverse to the number;

if the first estimated inverse is greater than the number, removing the first partial iteration of the result from the first register;

if the first estimated inverse is less than the number, [[:]] storing the first estimated inverse in a second register and leaving the first partial iteration in the first register;

wherein the first register stores a first result with a first resolution, wherein the second register stores an incremental effect of the first result;

~~determining~~ storing a ~~first~~ second partial iteration in the first register;

determining an incremental effect of the ~~first~~ second partial iteration on the inverse arithmetic function ~~as applied to the first partial iteration plus the first result~~;

adding the incremental effect of the second partial iteration to the ~~first estimated inverse~~ incremental effect of the first result to provide a second estimated inverse; and

comparing the second estimated inverse to the number;

if the second estimated inverse is greater than the number, removing the first partial iteration of the result from the first register; and

if the second estimated inverse is less than the number, storing the second estimated inverse in the second register and leaving the second partial iteration in the first register;

wherein the first register stores a second result with a second resolution greater than the first resolution, wherein the second register stores an incremental effect of the first result and the second result.

7. (original) The method of claim 6, wherein the arithmetic function is square root.

8. (currently amended) The method of claim 7, wherein the incremental effect <u>of the second partial iteration</u> comprises two times the first estimated inverse times the ~~first~~ <u>second</u> partial iteration plus the ~~first~~ <u>second</u> partial iteration squared.

9. (currently amended) The method of claim 8, wherein determining the ~~first~~ <u>second</u> partial iteration comprises shifting a one by a predetermined amount.

10. (currently amended) The method of claim 9, wherein determining the incremental effect <u>of the second partial iteration</u> comprises:

determining two times the first estimated inverse by shifting the first estimated inverse by one;

adding the first partial iteration to two times the first estimated inverse to provide a first inverse sum; and

multiplying the first inverse sum by the first partial iteration by shifting the first inverse sum by the predetermined amount.

11. (original) The method of claim 10, wherein the square root is of the number.

12. (original) The method of claim 6, wherein the arithmetic function is division.

13. (currently amended) The method of claim 12, wherein the incremental effect <u>of the second partial iteration</u> comprises one half the first <u>partial</u> iteration times the divisor.

14. (original) The method of claim 13, wherein performing an inverse function on the first iteration comprises shifting the divisor by predetermined amount.

15. (currently amended) The method of claim 14, wherein determining the incremental effect <u>of the second partial iteration</u> comprises shifting the divisor by an amount equal to the predetermined amount minus one.

16. A circuit for performing an arithmetic function applied to a number and provide a result of the arithmetic function based on partial iterations, comprising:

a counter for providing a count to identify a current partial iteration;

a comparator having a first input for receiving the number, a second input, and an output;

register means, having a first input coupled to the output of the comparator, a second input coupled to the counter, and an output, wherein the register means is for storing a current estimate of the result of the arithmetic function as applied to the number based on previous partial iterations, for providing an output representative of a next partial iteration, and for updating the result based on the output of the comparator;

storage means for storing an inverse of the arithmetic function of the current estimate and having an output on which is provided the inverse of the arithmetic function of the current estimate of the result;

incremental means having an input coupled to the output of the register means for providing, on an output, an incremental effect, wherein the incremental effect is a value that when added to the inverse of the mathematical function of the ~~last~~ current estimate is equal to the inverse function of ~~a next estimate~~ current estimate plus the next partial interation; and

summing means, having an output coupled to the second input of the comparator, a first input coupled to the output of the storage means, a second input coupled to the incremental means, for providing on the output a sum of ~~adding~~ the incremental effect ~~to~~ and the inverse of the arithmetic function of the current estimate.

17. (original) The circuit of claim 16, wherein the arithmetic function is division by a divisor.

18. (original) The circuit of claim 17, wherein the incremental means comprises:

a programmable shifter having a first input for receiving the divisor, a second input for receiving a signal indicating a shift amount, and an output coupled to the summing means.

19. (canceled)

20. (original) The circuit of claim 16, wherein the arithmetic function is square root.

21. (original) The circuit of claim 20, wherein the incremental means comprises:
    means for providing a signal having a value of two times the current estimate;
    means for generating a signal having a value of an incremental increase equal to the difference between the current estimate and the next estimate;
    means for summing two times the current estimate and the incremental increase; and
    means for multiplying the sum of the current estimate and the incremental increase by the incremental increase to generate the incremental effect.

22. (original) The circuit of claim 20, wherein the incremental means comprises:
    a first shifter for providing an output of a shift of a one by a predetermined amount;
    a second shifter for providing an output of a shift of the current estimate by one;
    a summer for providing an output of a sum of the outputs of the first and second shifters;
    a third shifter for providing an output of a shift of the predetermined amount of the output of the summer to the summing means.

23. (canceled)